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Date: March 27, 2006

Brooke French

In re application of: **Handgen, et al**

Confirmation No.: **8717**

U.S. Application Number: **10/630,260**

Art Unit: **2111**

Filing Date: **July 30, 2003**

Examiner: **Dang, Khanh**

Our Reference Number: **50833-1230**

Title: **Integrated Circuit with a Scalable High-Bandwidth Architecture**

Appeal Brief

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HEWLETT-PACKARD COMPANY
Intellectual Property Administration
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PATENT APPLICATION

ATTORNEY DOCKET NO. 200205911-1

IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Handgen, et al

Confirmation No.: 8717

Application No.: 10/630,260

Examiner: Dang, Khanh

Filing Date: July 30, 2003

Group Art Unit: 2111

Title: Integrated Circuit with a Scalable High-Bandwidth Architecture

Mail Stop Appeal Brief-Patents
Commissioner For Patents
PO Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL OF APPEAL BRIEF

Transmitted herewith is the Appeal Brief in this application with respect to the Notice of Appeal filed on February 20, 2006.

The fee for filing this Appeal Brief is (37 CFR 1.17(c)) $500.00.

(complete (a) or (b) as applicable)

The proceedings herein are for a patent application and the provisions of 37 CFR 1.136(a) apply.

☐ (a) Applicant petitions for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)-(d)) for the total number of months checked below:

☐ 1st Month $120 ☐ 2nd Month $450 ☐ 3rd Month $1020 ☐ 4th Month $1590

☐ The extension fee has already been filed in this application.

☒ (b) Applicant believes that no extension of time is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

Please charge to Deposit Account 08-2025 the sum of $ 500. At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account 08-2025 pursuant to 37 CFR 1.25. Additionally please charge any fees to Deposit Account 08-2025 under 37 CFR 1.16 through 1.21 inclusive, and any other sections in Title 37 of the Code of Federal Regulations that may regulate fees. A duplicate copy of this sheet is enclosed.

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Respectfully submitted,

By

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Rev 10/05 (ApiBrief)

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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:	
Handgen, et al	Group Art Unit: 2111 Examiner: Dang, Khanh
Serial No.: 10/630,260	Confirmation No. 8717
Filed: July 30, 2003	TKHR Dkt. No. 50833-1230 HP Docket No. 200205911-1
For: INTEGRATED CIRCUIT WITH A SCALABLE HIGH-BANDWIDTH ARCHITECTURE	

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Brooke French

APPEAL BRIEF UNDER 37 C.F.R. §1.192

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Sir:

This is an appeal from the decision of Examiner Khanh Dang, Group Art Unit 2111, mailed November 21, 2005, rejecting claims 1-12 in the present application and making the rejection FINAL.

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I. REAL PARTY IN INTEREST

The real party in interest of the instant application is Hewlett-Packard Development Company, a Texas Limited Liability Partnership having its principal place of business in Houston, Texas.

II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences.

III. STATUS OF THE CLAIMS

Claim 1-12 are pending in this application, and all claims were rejected by the FINAL Office Action and are the subject of this appeal.

IV. STATUS OF AMENDMENTS

All claim amendments submitted before the mailing date of the FINAL Office Action have been entered, and no claim amendments have been submitted subsequent to the mailing of the FINAL Office Action. In response to the FINAL Office Action, Applicant submitted a non-substantive amendment to the specification. A copy of the current claims is attached hereto as Appendix A.

V. SUMMARY OF CLAIMED SUBJECT MATTER

Embodiments of the claimed subject matter are illustrated in FIGs. 2 through 7 and are discussed in the specification at least at pages 5-14.

Embodiments of the invention, such as those defined by claim 1, define an integrated circuit component (see e.g., FIG. 6, reference number 410, and related description) comprising a logic block (see e.g., reference number 415a, and related description) capable of being configured to interface with a first companion integrated circuit (see e.g., reference number 210, and related description) and to receive information that is communicated from the first companion integrated circuit (see e.g., reference number 210, and related description), which information was communicated to the first companion integrated circuit via a first portion of a system bus (see e.g., reference number 105, and related description). The integrated circuit component (see e.g., reference number 410, and related description) further comprises a logic block (see e.g., reference number 415b, and related description) capable of being configured to interface with a second companion integrated circuit (see e.g., reference number 211, and related description) and to receive information that is communicated from the second companion integrated circuit, which information was communicated to the second companion integrated circuit (see e.g., reference number 211, and related description) via a second portion of the system bus (see e.g., reference number 105, and related description), wherein the first companion integrated circuit (see e.g., reference number 210, and related description) and the second companion integrated circuit (see e.g., reference number 211, and related description) are disposed in separate integrated circuit chips.

Embodiments of the invention, such as those defined by claim 6, define a system in which a plurality of companion integrated circuit components collectively implement a logic function embodied in a single, conventional integrated circuit component, comprising a host integrated circuit component (see e.g., FIG. 6, reference number 102, and related description) communicating with other integrated circuit components via a system bus (see e.g., reference

number 105, and related description). The system further comprises a first integrated circuit component (see e.g., reference number 210, and related description) comprising logic (see e.g., reference number 214, and related description) for interfacing with a first portion of system bus (see e.g., reference number 105, and related description), a second integrated circuit component (see e.g., reference number 211, and related description) comprising logic (see e.g., reference number 214, and related description) for interfacing with a second portion of system bus (see e.g., reference number 105, and related description), and a third integrated circuit component (see e.g., reference number 410, and related description) not directly coupled with the system bus and comprising logic (see e.g., reference numbers 415a, 515b, and related description) for communicating with the host integrated circuit (see e.g., reference number 102, and related description) via the first and second integrated circuit components (see e.g., reference numbers 210 and 211, and related description), wherein the first integrated circuit component, the second integrated circuit component, and the third integrated circuit component are provided in separate integrated circuit chips.

Embodiments of the invention, such as those defined by claim 9, define an integrated circuit component (see e.g., FIG. 6, reference number 410, and related description) comprising a first set of conductive pins (see specification, p. 14, paragraph 40) for channeling communications to a host integrated circuit (see e.g., reference number 102, and related description) through a first intermediate integrated circuit (see e.g., reference number 210, and related description), the first intermediate integrated circuit being in direct communication with the host integrated circuit (see e.g., reference number 102, and related description) via a first portion of a system bus (see e.g., reference number 105, and related description). The integrated circuit further comprises a second set of conductive pins (see specification, p. 14, paragraph 40)

for channeling communications to the host integrated circuit through a second intermediate integrated circuit (see e.g., reference number 211, and related description), the second intermediate integrated circuit being in direct communication with the host integrated circuit (see e.g., reference number 102, and related description) via a second portion of the system bus (see e.g., reference number 105, and related description), wherein the integrated circuit component, the first intermediate integrated circuit and the second intermediate integrated circuit are provided in separate integrated circuit chips.

Embodiments of the invention, such as those defined by claim 11, define an integrated circuit component (see e.g., FIG. 2, reference number 210, and related description) comprising two independent logic portions (see e.g., reference numbers 214 and 215, and related description), each logic portion being capable of being alternatively configured to communicate with a host integrated circuit (see e.g., reference number 102, and related description) via a portion of a system bus (see e.g., reference number 105, and related description) and a companion integrated circuit (see e.g., reference number 211, and related description) and to receive information that is communicated from the companion integrated circuit (see e.g., reference number 211, and related description), which information was communicated to the companion integrated circuit via a portion of a system bus (see e.g., reference number 105, and related description).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The Office Action rejected claim 7 under 35 U.S.C. § 112, second paragraph alleging that the phrase "at least one additional integrated circuit component" is indefinite.

The Office Action also rejected claim 11 as allegedly indefinite, stating that the work "alternatively" renders the claim indefinite.

The Office Action rejected claims 1-6 and 8-12 under 35 U.S.C. § 102(b) as allegedly anticipated by U.S. patent 6,172,906 (hereafter the '906 patent).

VII. ARGUMENT

Discussion of Rejections Under 35 U.S.C. § 112, Second Paragraph

Claim 7

The Office Action rejected claim 7 under 35 U.S.C. § 112, second paragraph alleging that the phrase "at least one additional integrated circuit component" is indefinite. The undersigned respectfully submits that this phrase is not unclear or indefinite. As the Office Action has construed the phrase "integrated circuit" as used in claim 6 (without rejecting it as indefinite), then the undersigned presumes that the phrase "integrated circuit component" is clear and definite to the Examiner. This is preceded by the phrase "at least one additional." "At least one" simply means one or more. Therefore, the total phrase "at least one additional integrated circuit component" should be construed as one or more additional integrated circuit components. Claim 6, from which claim 7 depends, defines first and second integrated circuits. Therefore, claim 7 requires a total of at least three integrated circuits.

The Examiner has requested that the undersigned identify where the specification supports the subject matter for this claim. In this regard, the undersigned respectfully suggests

that the Examiner compare the diagrams of FIGs. 2 and 6 (and related discussion). FIG. 2 illustrates an embodiment having two integrated circuit chips 210 and 211, while FIG. 6 illustrates an embodiment having "at least one additional integrated circuit component" 410. (See specification paragraphs 0034 through 0038). Accordingly, for at least this reason, the indefiniteness rejection of claim 7 should be overturned.

As claim 7 has not been rejected by the Office Action based on any prior art, Applicants submit that claim 7 is in immediate condition for allowance.

Claim 11

The Office Action also rejected claim 11 as allegedly indefinite, stating that the word "alternatively" renders the claim indefinite. Applicant disagrees. Alternative claiming does not *per se* render a claim indefinite. In fact, MPEP 2173.05(h) addresses this very issue stating:

> II. "OR" TERMINOLOGY
>
> Alternative expressions using "or" are acceptable, such as "wherein R is A, B, C, or D." The following phrases were each held to be acceptable and not in violation of 35 U.S.C. 112, second paragraph in In re Gaubert, 524 F.2d 1222, 187 USPQ 664 (CCPA 1975): "made entirely or in part of"; "at least one piece"; and "iron, steel or any other magnetic material."
>
> III. "OPTIONALLY"
>
> An alternative format which requires some analysis before concluding whether or not the language is indefinite involves the use of the term "optionally." In *Ex parte Cordova*, 10 USPQ2d 1949 (Bd. Pat. App. & Inter. 1989) the language "containing A, B, and optionally C" was considered acceptable alternative language because there was no ambiguity as to which alternatives are covered by the claim. A similar holding was reached with regard to the term "optionally" in *Ex parte Wu*, 10 USPQ2d 2031 (Bd. Pat. App. & Inter. 1989). In the instance where the list of potential alternatives can vary and ambiguity arises, then it is proper to make a rejection under 35 U.S.C. 112, second paragraph, and explain why there is confusion.

For at least this reason, the rejection of claim 11 should be overturned.

Further, Applicants submit that the rejection should be overturned, as the U.S. Patent & Trademark Office routinely issues patent claims that embody this same language. In fact, the undersigned performed an electronic search of the U.S. PTO patent database for patents having claims that include the term "alternatively" and according to the PTO Web site, some 19,253 patents have been issued with this language in their claims. As an example, U.S. Patent 6,980,810 was issued on December 27, 2005. Claim 12 of that patent recites:

> 12. An access point for use in a wireless local area network, said access point comprising:
> a processor for assigning a communication channel to a wireless station, said communication channel having a frequency and a spreading code associated therewith;
> said processor also for determining whether said wireless station is located in a first area which overlaps with another cell or in a second area which is non-overlapping with respect to said another cell; and
> a transmitter for transmitting information to said wireless station during a first portion of a superframe if said wireless station is located in said first area and, ***alternatively***, during a second portion of said superframe ***if said wireless station is located in said second area, transmitter also transmits a beacon signal containing information associated with a duration of said first and second portions of said superframe;***
> a receiver for receiving a beacon signal from said other cell and using, in said processor, information in said beacon signal to determine said duration of said first and second portions of said superframe.

(*Emphasis added.*) As can be readily verified from the above-quoted claim, the PTO is issuing patent with claims embodying the term "alternatively" as used in the same type of context of pending claim 11. Such a contextual use is clear and definite, and the rejection of claim 11 should be overturned.

In fact, even Examiner Khanh Dang (the Examiner of the present application) has issued a number of patents having claims containing the term "alternatively." As one example, U.S. Patent 6,566,839 was issued by Examiner Dang, and claim 5 of this patent recites:

> 5. The circuit of claim 2 wherein a plurality of additional capacitors are provided that are ***alternatively*** switched into series with said motor by said processor when the frequency of rotation of said rotor is greater than the resonant frequency of the previous capacitor and the reactance from the motor itself has again begun to prevent current from reaching the motor such that said subsequent capacitor resonates in a reinforcing manner with a higher frequency of said rotor.

For at least the foregoing reasons, the rejection of claim 11 should be overturned.

Having said this, the undersigned is agreeable to an Examiner's amendment that deletes the term "alternatively." The undersigned considered submitting such an amendment in a prior response, but was concerned that ANY amendment to the claims might result in an Advisory Action, alleging that the amendment raises new issues.

In view of the foregoing, Applicants respectfully submit that all claims, as amended, fully comply with the requirements of 35 U.S.C. § 112, second paragraph, and Applicants respectfully request that the rejections thereof be overturned.

Discussion of Rejections Under 35 U.S.C. § 102

Claim 1

The Office Action rejected claims 1-6 and 8-12 under 35 U.S.C. § 102(b) as allegedly anticipated by the '906 patent. For at least the reasons set forth below, Applicants respectfully disagree and request that the rejections be overturned. With regard to claim 1, claim 1 recites:

> 1. An ***integrated circuit component*** comprising:
> a logic block capable of being ***configured to interface with a first companion integrated circuit*** and to receive information that is communicated from the first companion integrated circuit, which information ***was communicated to the first companion integrated circuit via a first portion of a system bus***; and

> a logic block capable of being ***configured to interface with a second companion integrated circuit*** and to receive information that is communicated from the second companion integrated circuit, which information ***was communicated to the second companion integrated circuit via a second portion of the system bus, wherein the first companion integrated circuit and the second companion integrated circuit are disposed in separate integrated circuit chips.***

(*Emphasis added*). Applicants respectfully submit that claim 1 patently defines over the '906 patent for at least the reasons that the '906 patent fails to disclose the features emphasized above.

Notably, claim 1 is directed to "an integrated circuit component" (i.e., a single component) that includes two separate logic blocks. A first logic block is capable of being configured to interface with a first companion integrated circuit and to receive information that is communicated from the first companion integrated circuit, which information was communicated to the first companion integrated circuit via a first portion of the system bus. Likewise, the second logic block is capable of being configured to interface with a second companion integrated circuit and to receive information that is communicated from the second companion integrated circuit, which information was communicated to the second companion integrated circuit via a second portion of the system bus. Simply stated, these features are not disclosed in the '906 patent.

To assist in a better understanding of claim 1, consider the embodiment of Fig. 6 of the present application. The first companion integrated circuit corresponds to reference numeral 210, while the second companion integrated circuit corresponds to reference numeral 211. The first logic block corresponds to split bus logic 415a, while the second logic block corresponds to split bus logic 415b. As is illustrated in Fig. 6, and more particularly claimed in claim 1, the first logic block (e.g., split bus logic 415a) is capable of being configured to interface with a first companion integrated circuit 210 and to receive information that is communicated from the first companion integrated circuit via a first portion of a system bus 105. Likewise, the second logic block (e.g.,

split bus logic 415 b) is configured to communicate and receive information that is communicated over a second portion of a system bus and routed through the second companion integrated circuit 211.

Similarly, claim 1 also covers the embodiment of FIG. 2. In this regard, the first companion integrated circuit corresponds to reference numeral 210, while the second companion integrated circuit corresponds to reference numeral 211. The first logic block corresponds to the split logic block 214 of component 210, while the second logic block corresponds to split bus logic 215 of component 211.

The teachings applied by the Office Action from the '906 patent (disclosing two memory chips 670 and 672 of a memory bank 506) are simply inapplicable to the embodiments of the invention as defined by claim 1. For at least this reason, the rejection of claim 1 should be overturned.

Claim 2-5

As claims 2-5 depend from claim 1, the substantive rejections of those claims should be overturned for at least the same reasons. In addition, each rejection of these claims merely alleges that the claimed subject matter is clearly taught in the '906 patent. For example, the rejection of claim 2 states that "it is clear that the controller (12/510) provides unified bus logic configured to consolidate information received from both logic portions." Applicants disagree. Reference number 510 of the '906 patent is merely a block labeled as "controller." The undersigned respectfully submits that this controller can operate in accordance with a prior art "memory controller" as summarized in the background section of the present application (see paragraph 003).

As such, the claimed feature is not inherent in the cited element, and the rejection is misplaced and should be withdraw.

In addition, the Examiner has taken the position that the I/O register 22/32 or 671/673 of the '906 patent is readable on the claim "logic block." (Office Action, p. 9) However, this application of the '906 patent is inconsistent the application of the '906 patent to claim 2. In this regard, claim 2 specifies that the claimed integrated circuit further comprises "a unified bus logic block configured to consolidate information received from both logic blocks." The controller 12/510 does not consolidate the information received from the I/O registers 22/32 or 671/673. For at least this additional reason, the rejection of claim 2 should be overturned.

For similar reasons, Applicants submit that the rejections of claims 3-5 should be overturned for at least the same reasons. The Examiner has maintained these rejections, despite the undersigned's prior requests that the Examiner indicate, with particularlity, where the claimed features are disclosed in the '906 patent.

Claim 6

With regard to independent claim 6, claim 6 recites:

> 6. A system in which a plurality of companion integrated circuit components collectively implement a logic function embodied in a single, conventional integrated circuit component, comprising:
> a host integrated circuit component communicating with other integrated circuit components via a system bus;
> a first integrated circuit component comprising logic for interfacing with a first portion of system bus;
> a second integrated circuit component comprising logic for interfacing with a second portion of system bus;
> a third integrated circuit component not directly coupled with the system bus and comprising logic for communicating with the host integrated circuit via the first and second integrated circuit components, ***wherein the first integrated circuit component, the second integrated circuit component, and the third***

integrated circuit component are provided in physically separate integrated circuit chips.

(*Emphasis added*). Applicants respectfully submit that claim 6 defines over the '906 patent for at least the reasons that the '906 patent fails to teach those features emphasized above.

As amended, claim 6 specifies that the first integrated circuit component and the second integrated circuit component are separate integrated circuit chips. As described in the specification of the present application, one benefit of the present invention is realized through the reduction in pin count on integrated circuit packages by distributing functionality across multiple integrated circuit packages, whereby each package may have certain conductive pins that interface with only a portion of the system bus (thereby reducing the pin count for a given IC chip). An embodiment covered by claim 6 includes a system comprising a host integrated circuit 102, a first integrated circuit component, a second integrated circuit component, and a third integrated circuit component. As previously described herein, claim 6 reads on the embodiment illustrated in Fig. 2, wherein the first integrated circuit component includes split bus logic 214 of component 210, whereas the second integrated circuit component includes split bus logic 214 of integrated circuit component 211. As is illustrated in the diagram of Fig. 2, integrated circuit components 210 and 211 are physically separate integrated circuit chips. The third integrated circuit component comprises split but logic 215 which, as illustrated, is not directly coupled with the system bus 105, but can nevertheless communicate with the host 102 by way of split bus logic 214.

Similarly, claim 6 reads on the embodiment illustrated in Fig. 6, wherein the third integrated circuit component may comprise either split bus logic 215 or split bus logic 415 (e.g., 415a and/or 415b).

Simply stated, the teachings of the '906 patent are not applicable to the embodiments defined by claim 6, as the '906 patent fails to disclose at least the third integrated circuit component. Specifically, claim 6 defines the first, second, and third integrated circuit components as comprising separate integrated circuit chips, and it is clear that the applied element (reference numeral 669 of the '906 patent) does not comprise a physically separate integrated circuit chip from reference numeral 670, which is applied as allegedly comprising the second integrated circuit component. Accordingly, the rejection of independent claim 6 should be overturned.

The Office Action further alleges that the '906 patent "discloses a third integrated circuit component (defined by flash storage 669 or 674) not directly coupled with the system bus (675)." (Office Action, p. 5). However, claim 6 expressly requires that the third integrated circuit is configured such that "***wherein the first integrated circuit component, the second integrated circuit component, and the third integrated circuit component are provided in physically separate integrated circuit chips.***"

The Office Action (pp. 10-11) cites a flash memory chip and a flash storage chip as comprising two such physically separate chips. However, such a controller/memory configuration is nothing more than Applicants characterized as prior art (see reference numbers 102 and 110 of FIG. 1). Significantly, the flash storage components 669 or 674 cited by the Office Action do not communicate "with the host via the first and second integrated circuit components," as specifically claimed by claim 6. For at least this

additional reason, the application of the '906 patent against the embodiment defined by claim 6 is misplaced and the rejection should be overturned.

Claim 8

As claim 8 depends from claim 6, the substantive rejections of this claim should be overturned for at least the same reasons. In addition, the rejection of claim 8 merely alleges that the claimed subject matter is clearly taught in the '906 patent (without specifically identifying where the claimed subject matter is taught). For example, the rejection of claim 8 states that "it is clear that the third integrated circuit further comprising functional logic (memory operation logic, for example) that performs a conventional functional operation (memory operation)." Applicants disagree.

For reasons similar to those set forth above in connection with claim 2, Applicants submit that the rejection of claim 8 is incomplete as failing to particularly point out relevant teaching of the '906 patent, and should be overturned for at least the same reasons.

Claims 9 and 10

With regard to independent claim 9, claim 9 is directed to an embodiment that reads on, for example, the embodiment illustrated in Fig. 6. Significantly, claim 9 is directed to an integrated circuit 410 that comprises two sets of conductive pins for channeling communications to a host integrated circuit 102 through two intermediate integrated circuits 210 and 211. The teachings of the '906 patent disclose a data bus that has a portion connected to a first flash memory 670 and a second portion of the data bus coupled to a second flash memory 672. Significantly, however, there

is no disclosure in the '906 patent of an integrated circuit that is coupled to a host integrated circuit via two intermediate integrated circuits, as is claimed in claim 9. More specifically, claim 9 recites:

> 9. An integrated circuit component comprising:
> a first set of conductive pins ***for channeling communications to a host integrated circuit through a first intermediate integrated circuit, the first intermediate integrated circuit being in direct communication with the host integrated circuit via a first portion of a system bus***; and
> a second set of conductive pins ***for channeling communications to the host integrated circuit through a second intermediate integrated circuit, the second intermediate integrated circuit being in direct communication with the host integrated circuit via a second portion of the system bus, wherein the integrated circuit component, the first intermediate integrated circuit and the second intermediate integrated circuit are provided in separate integrated circuit chips.***

The Office Action acknowledges that some of these features are not taught in the '906 patent, but alleges that they are inherent. In this regard, the Office Action states that "it is clearly inherent that flash memory (669/674) must comprise pins for providing electrical connections and communication ... for channeling communication to a host integrated circuit..." Applicant disagrees that the recited structure is "inherent" in the '906 patent. In this regard, claim 9 specifically recites "a first set of conductive pins for channeling communications to a host integrated circuit through a first intermediate integrated circuit ... and a second set of conductive pins for channeling communications to the host integrated circuit through a second intermediate integrated circuit ... the first intermediate integrated circuit and the second intermediate integrated circuit are provided in separate integrated circuit chips." As described in the specification (see e.g., paragraph 0040), the pin layout eliminates the need that each controller have two complete sets of pins.

For at least this reason, the application of the '906 as an anticipatory reference to claim 9 is misplaced, and the rejection should be overturned. Likewise, the rejection of claim 10, which depends from claim 9 should be overturned as well.

Claims 11 and 12

Finally, Applicants refer to independent claim 11, which is directed to an integrated circuit (see, e.g., Figs. 2-4) having two independent logic portions, with each logic portion being "alternatively configured to communicate with a host integrated circuit via a portion of the system bus and a companion integrated circuit..." There is no teaching whatsoever, in the '906 patent of logic portions that are configurable to alternatively communicate either directly with a host component (e.g., split bus logic 214 of Fig. 2) or to be configured to communicate with a companion integrated circuit (e.g., split bus logic 215 of Fig. 2). The Office Action appears to rely on the word "or" in the original claim as requiring "only one condition" in order for the prior art to meet the claim limitations. As previously amended, the term "or" has been removed from claim 11 and all claim limitations now must be considered. For at least the reasons stated above, claim 11 patently defines over the '906, and the rejection thereof should be overturned. For at least the same reason, the rejection of dependent claim 12 should be overturned as well.

CONCLUSION

Based upon the foregoing discussion, Applicant respectfully requests that the Examiner's final rejection of claims 1-12 be overturned by the Board, and that the application be allowed to issue as a patent with all pending claims 1-12.

Application of Handgen, et al.
Ser. No. 10/630,260

In addition to the claims of Appendix A, Appendix B attached hereto indicates that there is no evidence being attached and relied upon by this brief. Appendix C attached hereto indicates that there are no related proceedings.

Please charge Hewlett-Packard Company's deposit account 08-2025 in the amount of $500 for the filing of this Appeal Brief. No additional fees are believed to be due in connection with this Appeal Brief. If, however, any additional fees are deemed to be payable, you are hereby authorized to charge any such fees to deposit account No. 08-2025.

Respectfully submitted,

Daniel R. McClure
Registration No. 38,962

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VIII. CLAIMS - APPENDIX

1. An integrated circuit component comprising:

a logic block capable of being configured to interface with a first companion integrated circuit and to receive information that is communicated from the first companion integrated circuit, which information was communicated to the first companion integrated circuit via a first portion of a system bus; and

a logic block capable of being configured to interface with a second companion integrated circuit and to receive information that is communicated from the second companion integrated circuit, which information was communicated to the second companion integrated circuit via a second portion of the system bus, wherein the first companion integrated circuit and the second companion integrated circuit are disposed in separate integrated circuit chips.

2. The integrated circuit component of claim 1, further comprising a unified bus logic block configured to consolidate information received from both logic blocks.

3. The integrated circuit component of claim 1, further comprising a functional logic block for performing at least one logic operation for the integrated circuit component.

4. The integrated circuit component of claim 1, wherein the system bus is a point-to-point serial communication bus.

5. The integrated circuit component of claim 1, wherein the first portion of the system bus is substantially one-half of the system bus and the second portion of the system bus is a remainder of the system bus.

6. A system in which a plurality of companion integrated circuit components collectively implement a logic function embodied in a single, conventional integrated circuit component, comprising:

a host integrated circuit component communicating with other integrated circuit components via a system bus;

a first integrated circuit component comprising logic for interfacing with a first portion of system bus;

a second integrated circuit component comprising logic for interfacing with a second portion of system bus;

a third integrated circuit component not directly coupled with the system bus and comprising logic for communicating with the host integrated circuit via the first and second integrated circuit components, wherein the first integrated circuit component, the second integrated circuit component, and the third integrated circuit component are provided in separate integrated circuit chips.

7. The system of claim 6, further at least one additional integrated circuit component not directly coupled with the system bus, and comprising logic for communicating with the host integrated circuit via the first, second, and third integrated circuit components.

8. The system of claim 6, wherein the third integrated circuit further comprising a functional logic block that performs a conventional functional operation.

9. An integrated circuit component comprising:

a first set of conductive pins for channeling communications to a host integrated circuit through a first intermediate integrated circuit, the first intermediate integrated circuit being in direct communication with the host integrated circuit via a first portion of a system bus; and

a second set of conductive pins for channeling communications to the host integrated circuit through a second intermediate integrated circuit, the second intermediate integrated circuit being in direct communication with the host integrated circuit via a second portion of the system bus, wherein the integrated circuit component, the first intermediate integrated circuit and the second intermediate integrated circuit are provided in separate integrated circuit chips.

10. The integrated circuit component of claim 9, further comprising unified bus logic configured to consolidate information received from the channeled communications through the first and second set of conductive pins.

11. An integrated circuit component comprising two independent logic portions, each logic portion being capable of being alternatively configured to communicate with a host integrated circuit via a portion of a system bus and a companion integrated circuit and to receive information that is communicated from the companion integrated circuit, which information was communicated to the companion integrated circuit via a portion of a system bus.

12. The integrated circuit component of claim 11, further comprising a unified bus logic block configured to consolidate information received from both logic portions.

IX. EVIDENCE - APPENDIX

None.

IX. RELATED PROCEEDINGS- APPENDIX

None.